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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,204	09/01/2004	Robert J. Devins	BUR920030020US1	5203

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EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,204	DEVINS ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed on 15 September 2006 have been fully considered but they are not persuasive.

Regarding the primary reference [Gustafsson], on page 6 of applicant's remarks, applicant has presented the argument that Gustafsson fails to "disclose a single set of common instructions that are used to initialize each one of the processor. In fact, Gustafsson specifically uses a separate location for storing instructions for each one of the processor." Regarding the secondary reference [Boyd], applicant has not presented any argument as to why Boyd fails to anticipate, in whole or in part, any of applicant's claims.

Regarding the applicant's remarks concerning Gustafsson, the examiner respectfully disagrees. Gustafsson clearly teaches that there exists a single set of common instructions that are used to initialize each of the processors. Col. 6, lines 8-10 of Gustafsson reads:

"At start-up, all processors in the multiprocessing system execute the same code read in the WhoAmI register."

Additionally, Fig. 3 shows an exemplary listing of assembly code that can be used to initialize the system of Gustafsson. According to Fig. 3, a common set of assembly code is used to read the WhoAmI register and test to see if the booting processor corresponds to particular processing being tested for (e.g. instructions 104, 110, 116, and 122). From the remainder of the assembly instructions present and Gustafsson's disclosure at col. 6, line 32 to col. 7, line 28, it is clear that each of the booting processors execute this portion of code in order to determine its own identity. Once the identity is determined, the booting processor accesses and executes code particular to that processor. The code particular to that processor is located at a labeled memory location. For example, in instruction 108 in the section of code labeled

"jumpstation", the jump instruction jumps to a memory location storing code for processor 0 at location "cpu0" if the previous steps determine that the identity of the booting processor is processor 0. In instruction 114, the jump instruction jumps to a memory location storing code for processor 1 at location "cpu1" if the previous steps determine that the identity of the booting processor is processor 1. The remainder of the assembly code functions in a similar fashion.

Regarding applicant's amendments to the independent claims, the examiner notes that the amendments do not change the scope or clarity of what is being claimed, and merely offer an alternative wording to what has already been presented. For example, there is no substantial difference between claiming "unique instructions" and "specific instructions". Additionally, the new limitations introduced in claims 12 and 13 are already anticipated by Gustafsson.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8 and 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Gustafsson et al., U.S. Patent No. 6,701,429 B1.

Regarding claim 1, Gustafsson teaches a method of initializing a plurality of processors in an integrated circuit, the method comprising the steps of:

identifying each one of the processors ["WhoAmI register", col. 5, lines 57-66];

executing boot code for initializing each one of the processors, the boot code containing specific code for at least one of the processors and common code that is common for each one of the processors [Fig. 3], the specific code being accessed according to the identity of the processor executing the boot code [col. 6, lines 8-13, 32-50].

Gustafsson also teaches that the multiprocessor is embodied on an integrated circuit [on-chip multiprocessor, col. 4, lines 53-57].

Regarding claims 2 and 3, Gustafsson teaches that a unique value is assigned to a WhoAmI register for each processor [Fig. 3, code tests if WhoAmI register identifies as processor 1, 2, 3, etc].

Regarding claims 4-8, Gustafsson teaches the method of claims 1-3, and also teaches the apparatus with means to implement the claimed method, and the integrated circuit that implements the claimed method. Gustafsson also teaches that the integrated circuit comprises a bus and a memory.

Regarding claims 10 and 11, the limitations recited appear to be similar in scope to those recited in claims 1-3, and are rejected on similar grounds.

Regarding claims 12 and 13, Gustafsson teaches accessing the same memory location for each one of the processors when executing the single set of instructions [Fig. 3, all processors execute this code, col. 1, lines 34-42, shared memory system with single address space], and accessing a memory location that is different from that used to store the single set of instructions for the unique instructions [Fig. 3, locations for cpu0, cpu1, cpu2, etc].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gustafsson in view of Boyd et al., U.S. Patent No. 5,895,487.

Regarding claim 9, Gustafsson does not teach a cache shared between the plurality of processors.

Boyd teaches a single-chip multiprocessor system with a shared, integrated L1 and L2 cache [Fig. 10].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Gustafsson and Boyd by implementing the caching system taught by Boyd in the system of Gustafsson. Both Boyd and Gustafsson teach single-chip multiprocessor systems. Boyd discloses the known advantages of caching in his background disclosure [col. 1, lines 15-52], and teaches the additional benefits of his inventive teachings [col. 2, line 62 to col. 3, line 10]. It would have therefore been obvious to one of ordinary skill in the art that the teachings of Boyd could have been applied to the system of Gustafsson, resulting in the improvements disclosed by Boyd.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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